

FIG. 1

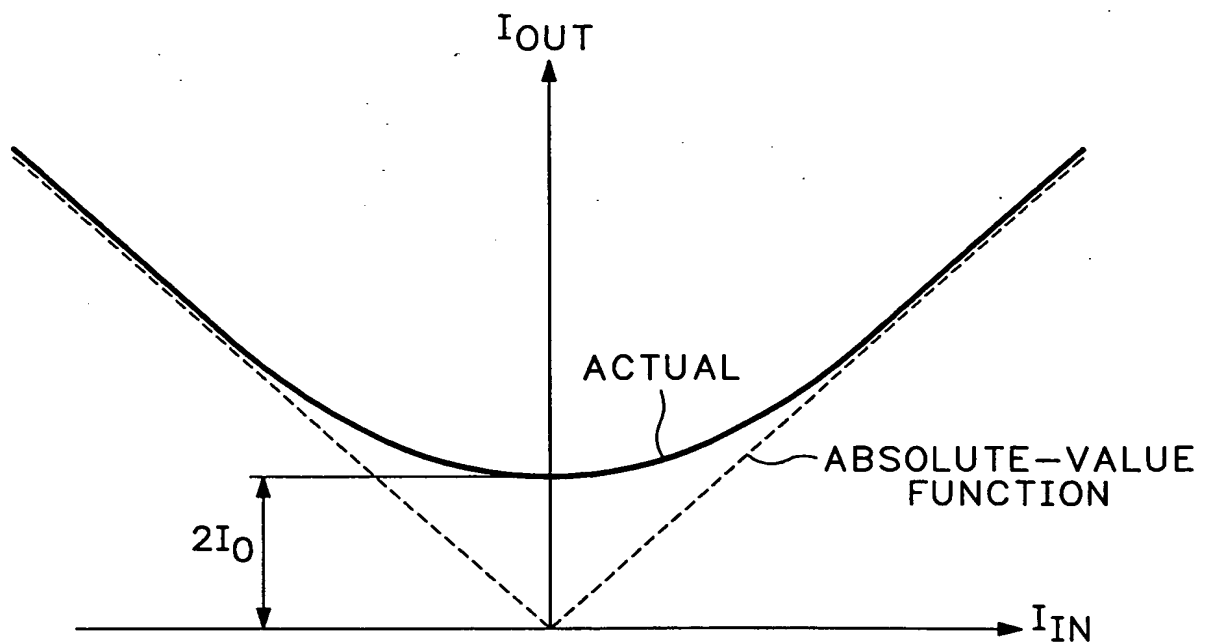


FIG. 2

FIG. 3

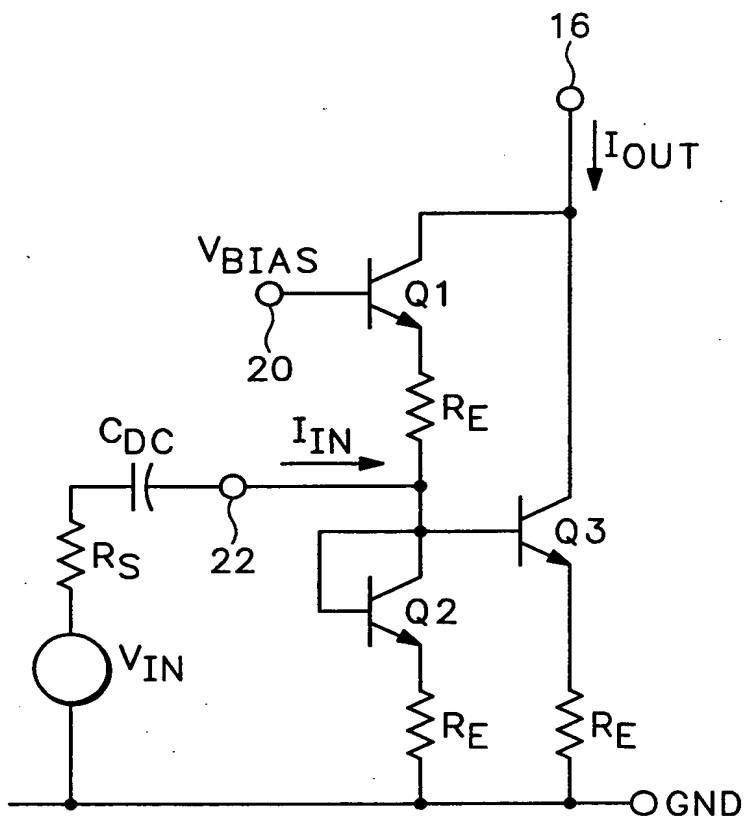


FIG.4

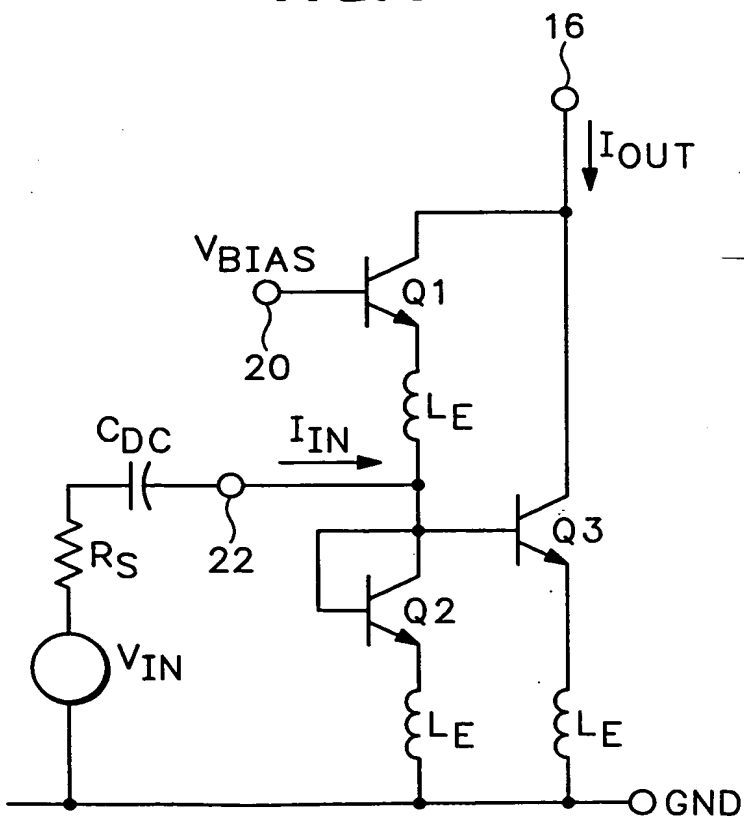


FIG.5

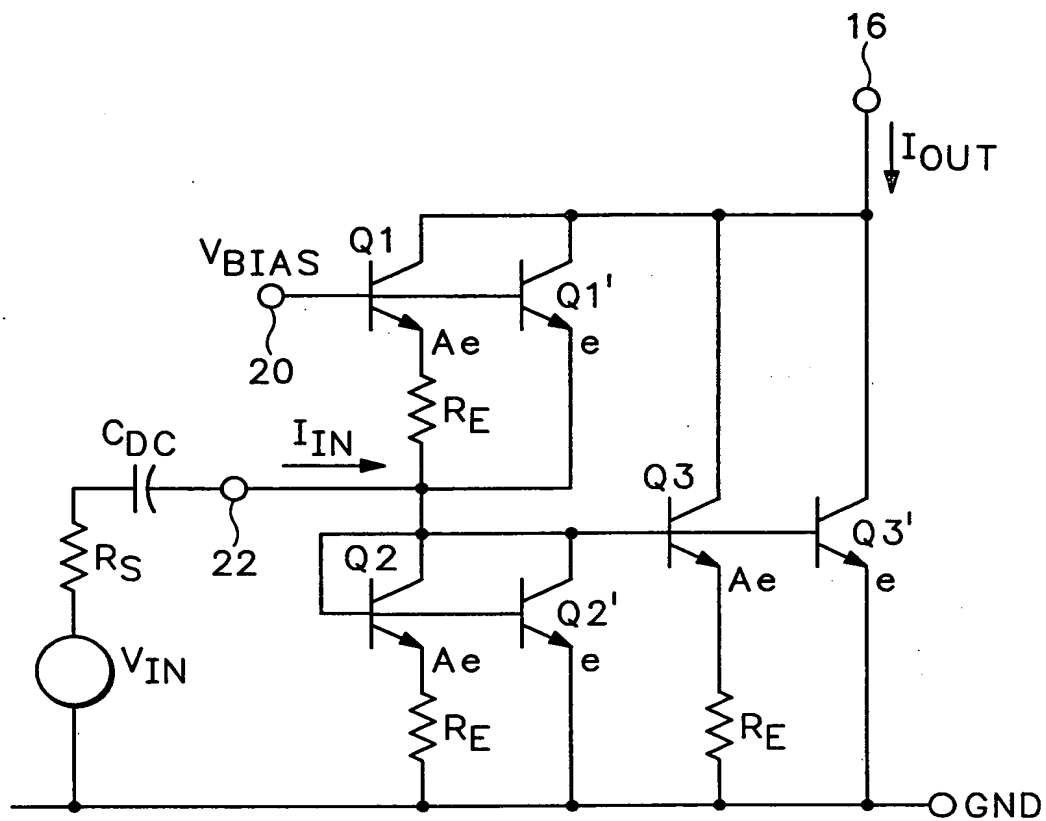


FIG.6

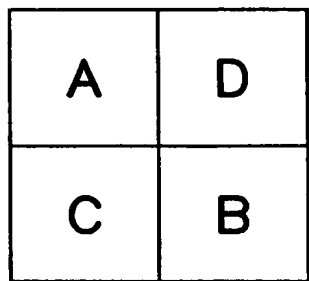


FIG.8

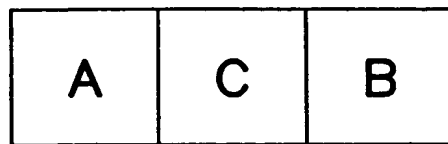


FIG.9

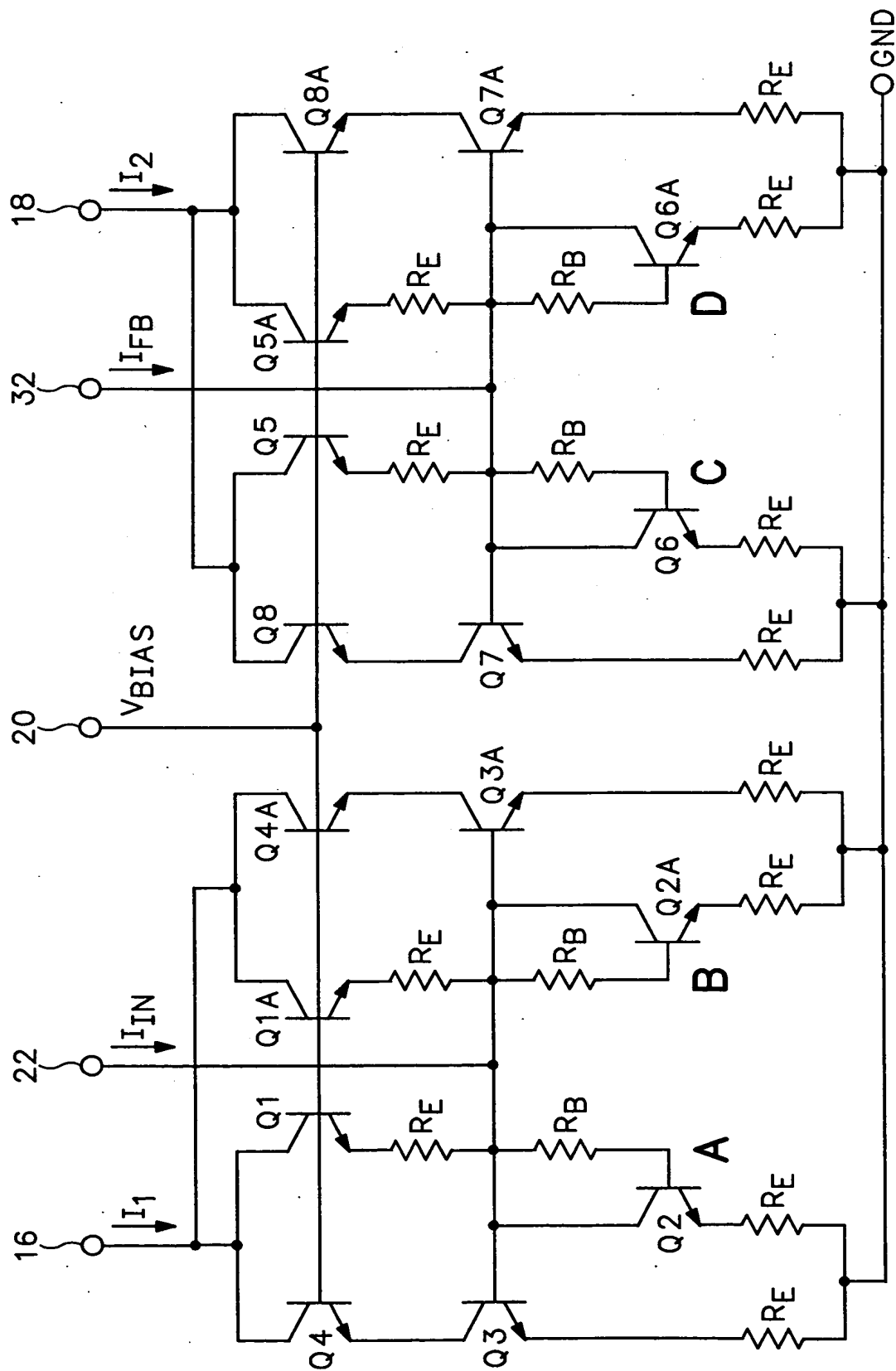
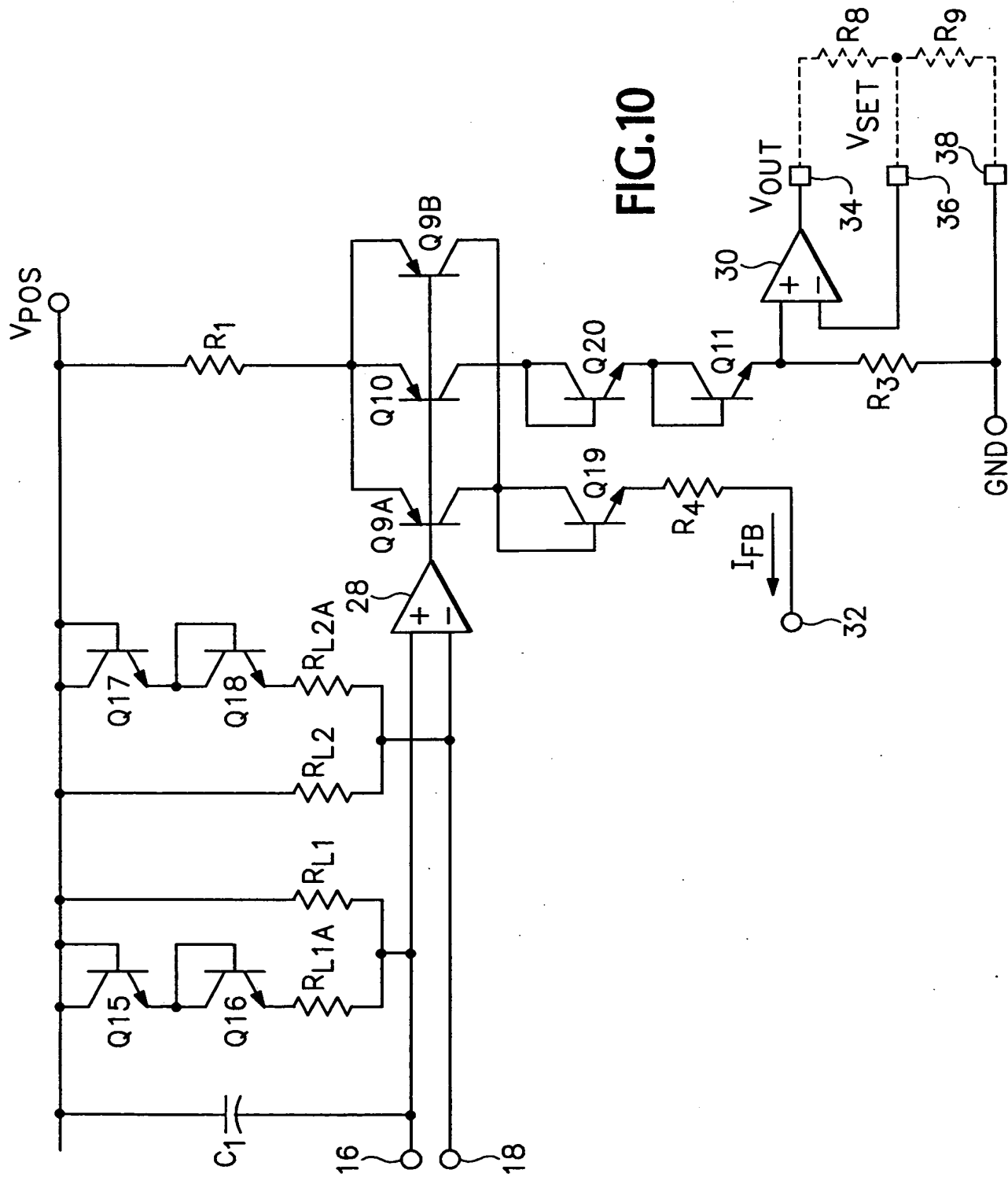


FIG.7



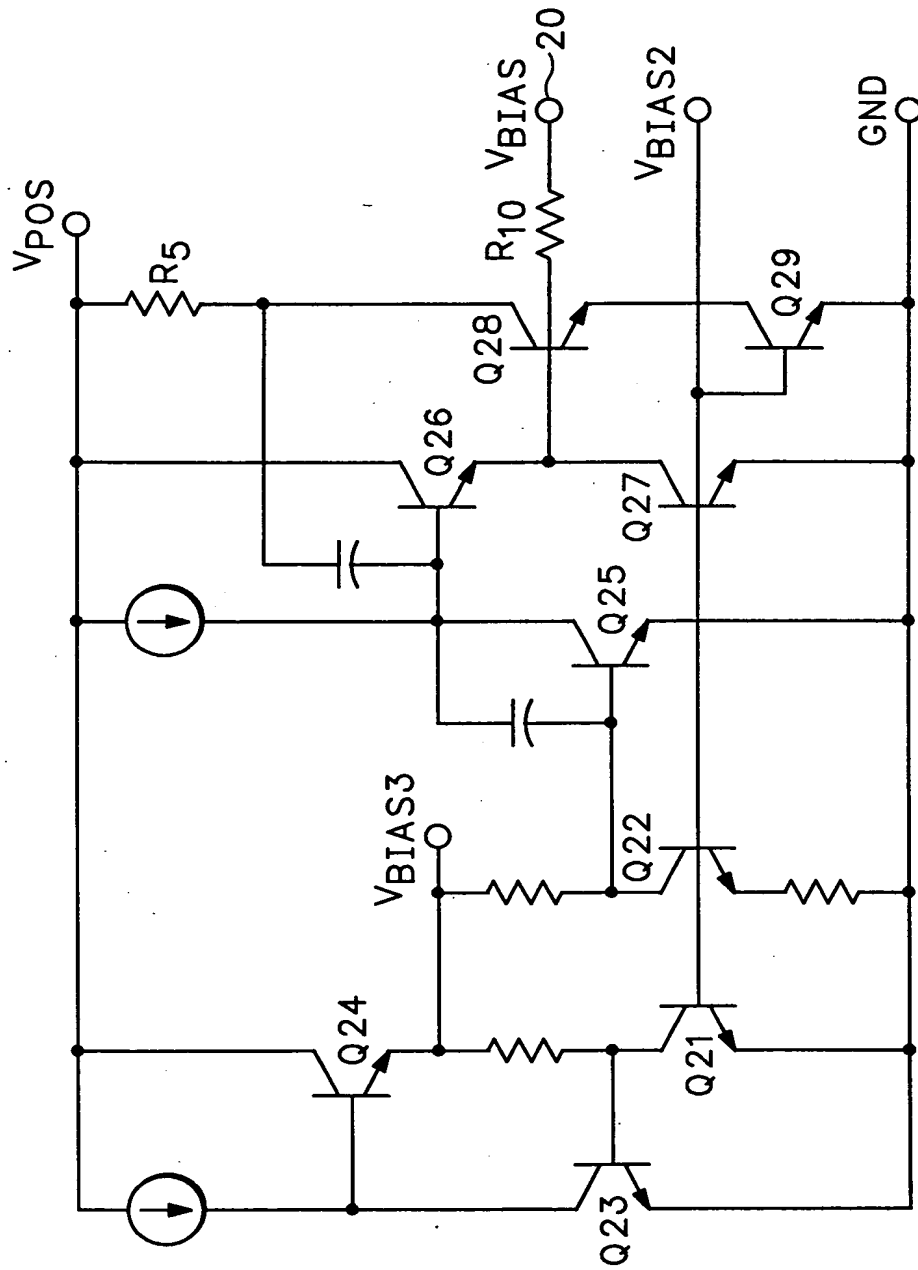
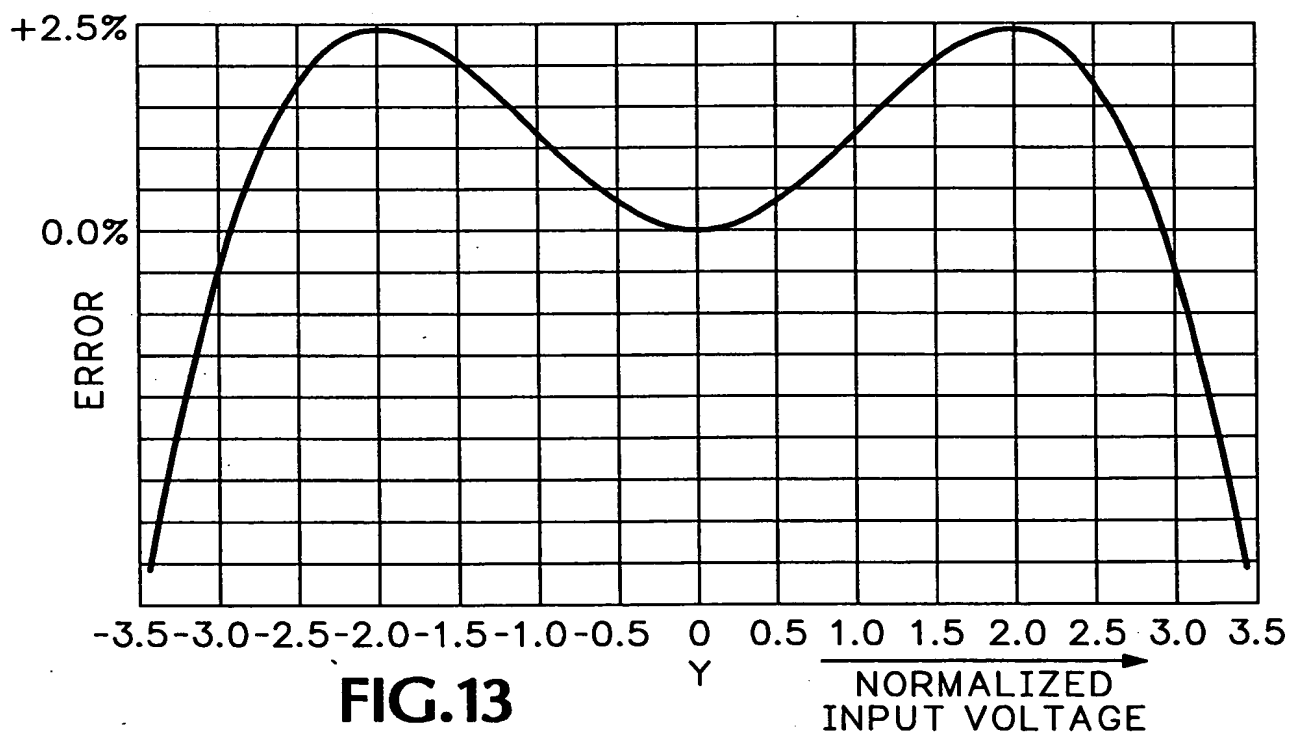
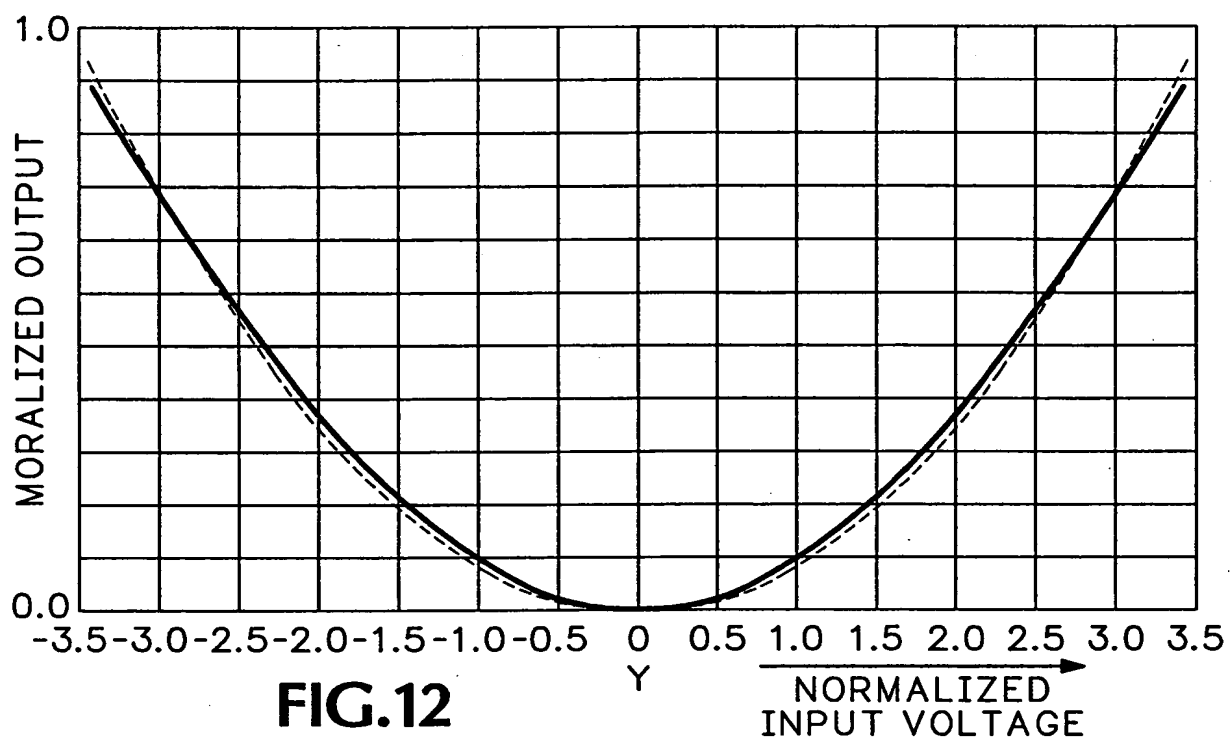
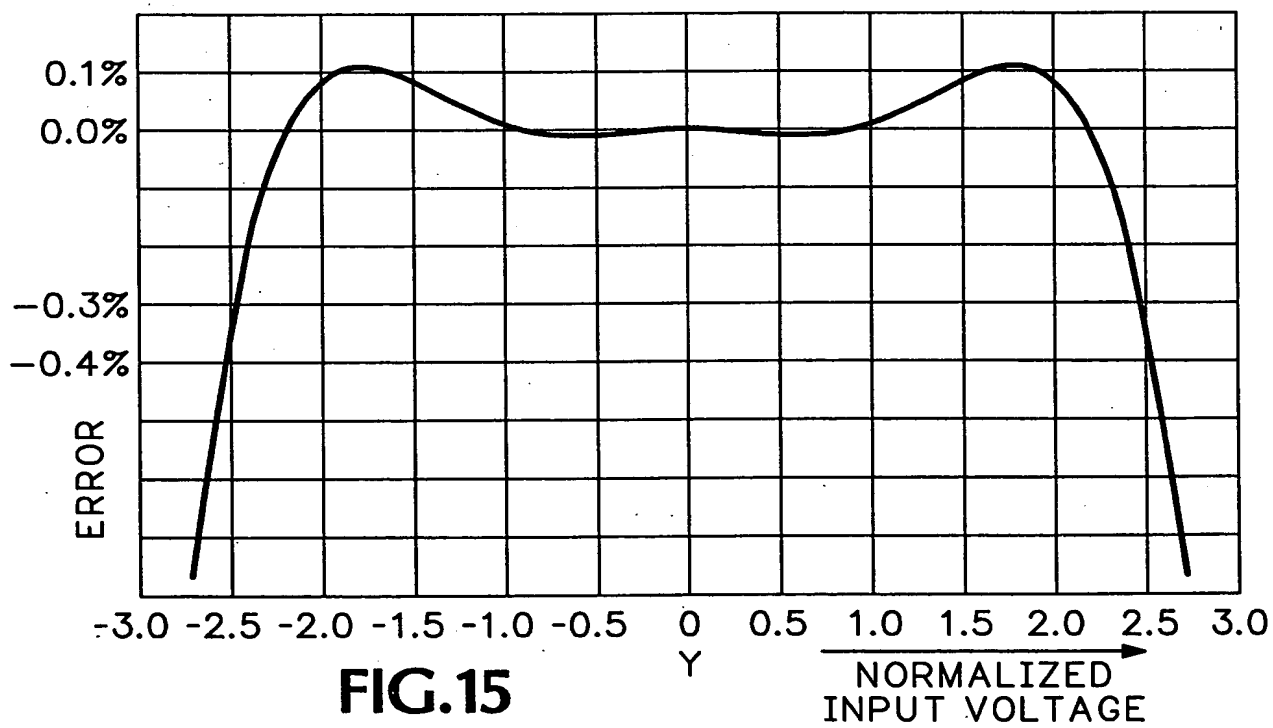
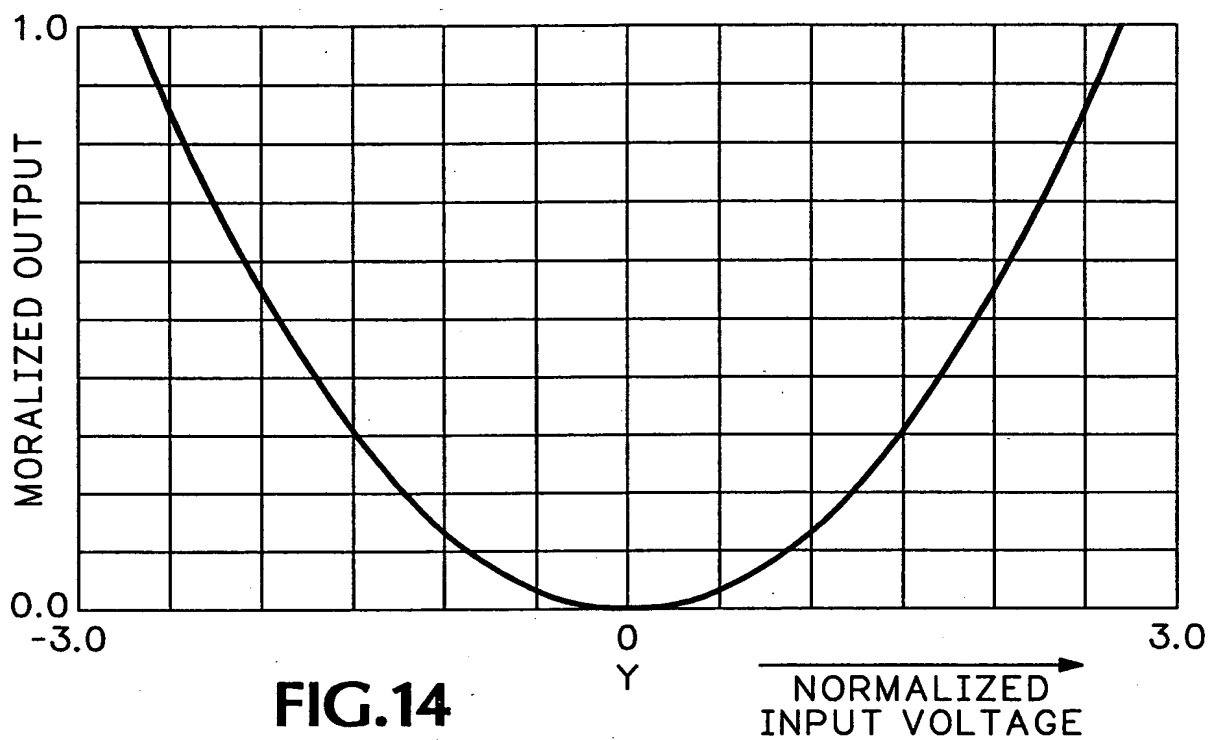


FIG.11

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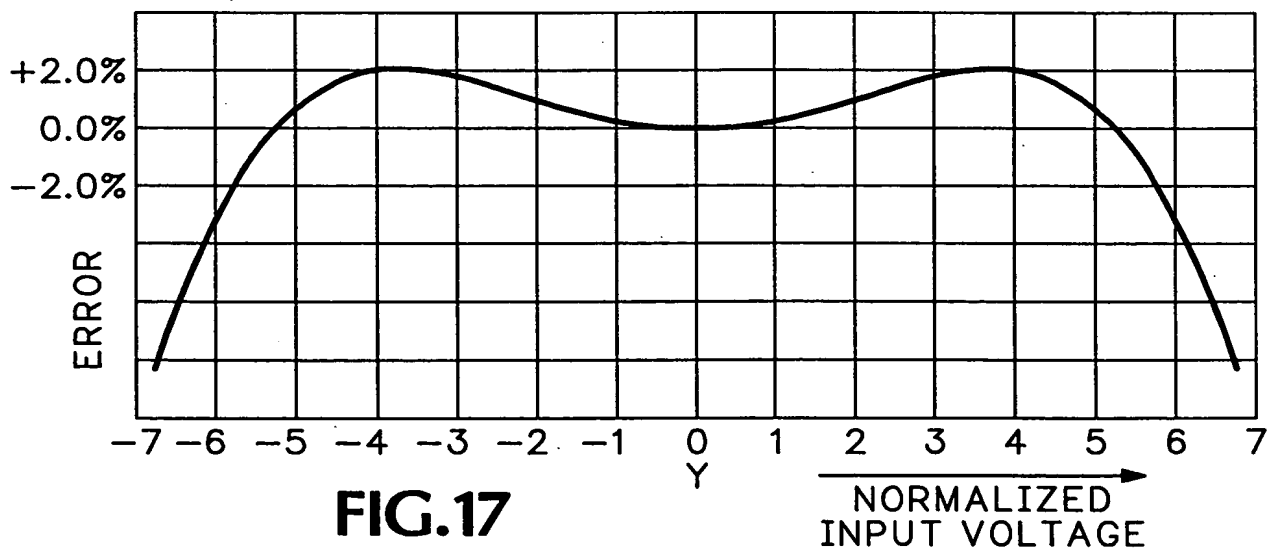
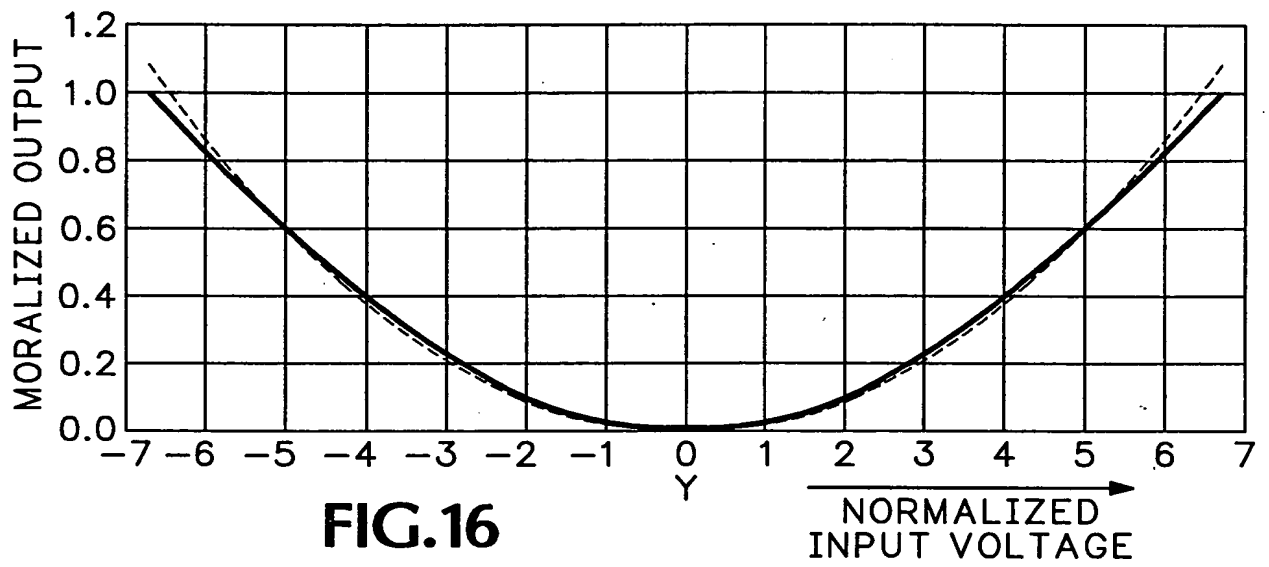


FIG. 18 is a circuit diagram of a differential amplifier. The circuit includes a differential pair of transistors, Q15 and Q17, with their emitters connected to a common emitter resistor network consisting of resistors RL1, RL2, RL1A, and RL2A. The bases of Q15 and Q17 are connected to a common base node, which is biased by a voltage divider network consisting of resistors R0 and R1, connected to a positive supply voltage VPOS. A capacitor C1 is connected between the base node and the common emitter resistor network. The collectors of Q15 and Q17 are connected to a common collector node, which is biased by a voltage divider network consisting of resistors R2 and R3, connected to VPOS. The output of the differential amplifier is taken from the collector node, which is connected to a load resistor RL2A and a differential-to-single-ended converter circuit, represented by a triangle symbol with a plus sign and a minus sign, and labeled 28. The input signals I1 and I2 are applied to the bases of Q15 and Q17, respectively, through terminals 16 and 18.

FIG.18